White Paper

Minimizing Ground Bounce & V_{CC} Sag

Introduction

Today's semiconductor market demands faster devices with more functionality and higher input/output (I/O) counts. Faster devices exhibit faster edge rates, which, if not properly used, can cause noise related problems. Also, increased I/O counts introduce more switching noise.

Two common noise-related analog phenomena encountered by digital designs are ground bounce and V_{CC} sag. Ground bounce and V_{CC} sag exist to some degree in almost every board. Normally, if ground bounce occurs on a board, V_{CC} sag occurs as well. The semiconductor industry is well aware of these phenomena and the effects they can have on high-speed applications.

Because programmable logic devices (PLDs) offer flexibility, they are ideal for solving noise-related problems such as ground bounce and V_{CC} sag. This white paper discusses ground bounce and V_{CC} sag, why they occur, and how Altera® PLDs can minimize these problems.

What Are Ground Bounce & V_{CC} Sag?

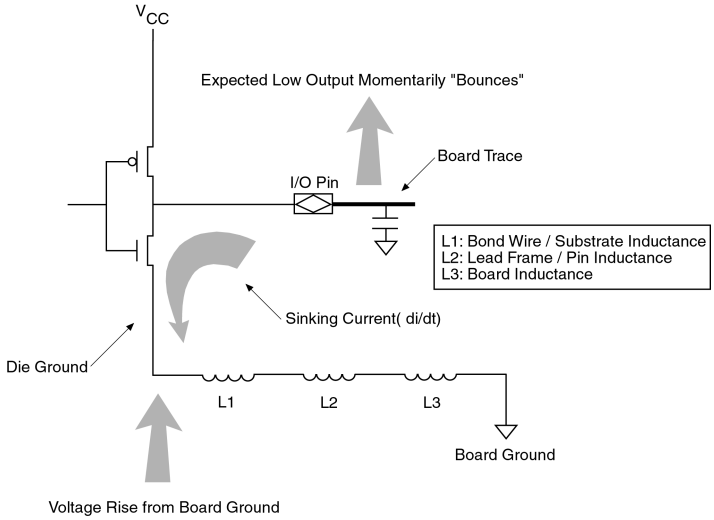
Many printed circuit boards (PCBs) have data buses running between devices with the bits of the bus placed adjacently to make debugging and routing the signals on the board easier. While this makes board and device design simpler, it can create some problems with signal integrity, including ground bounce and V_{CC} sag.

Ground Bounce

Ground bounce occurs when most, if not all, of the bits of the data bus simultaneously switch from `1` to `0`. During ground bounce, the device ground rises, or bounces, relative to the board ground. Figure 1 shows the connections between the board, the device, and the load and illustrates how the device ground bounces when the I/O pins switch from `1` to `0`.

Due to the inductance, a voltage is produced between the device ground and the board ground, which is proportional to the rate of change in current, or $V = L \times (di/dt)$.

Figure 1. How Ground Bounce Occurs

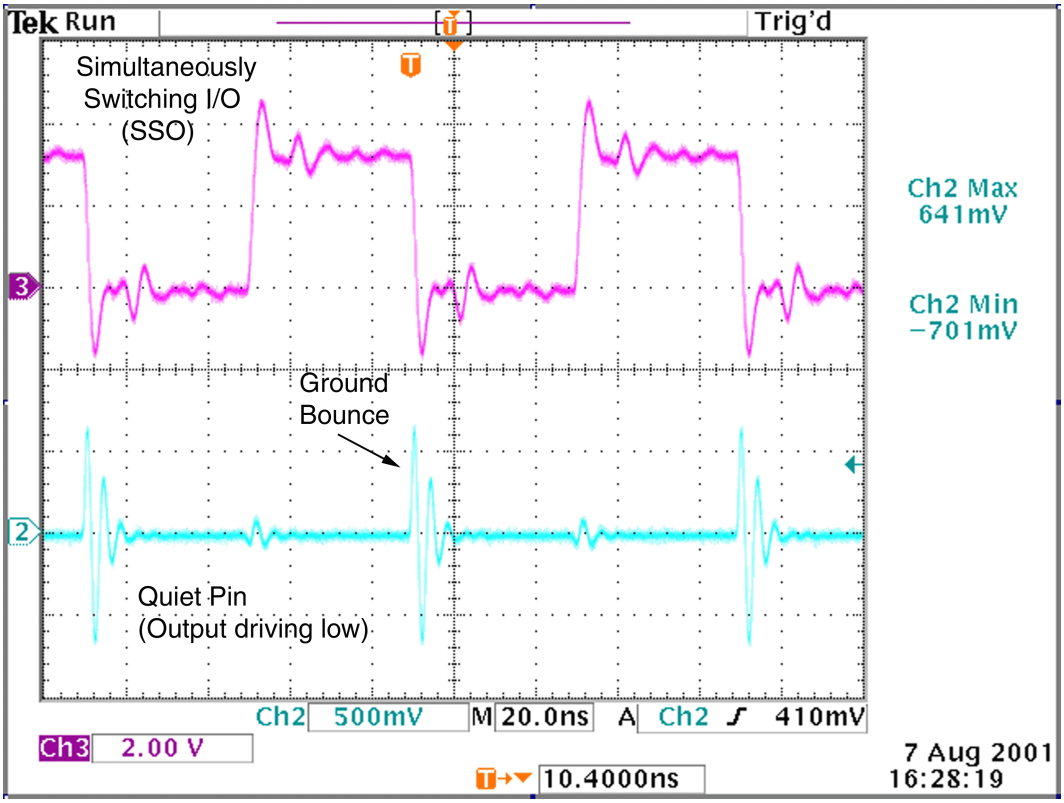


If the I/O pin is driving out a logic `1`, the load capacitor is charged. When this pin switches from `1` to `0`, a rush of current (di/dt) flows from the load capacitor through the I/O and the ground of the device to the board ground. This sudden rush of current (di/dt), in combination with the inductances (L) in the pin, device packaging, and connection to the board ground, causes a voltage difference to be generated between the board ground and the device ground. Because the sudden rush in current builds and then recedes, the ground of the device bounces.

The ground bounce amplitude increases with the number of simultaneously switching outputs (SSOs) switching from high to low as well as the load capacitance. A larger load capacitance provides more charge and, hence, more current. Each additional SSO draws more current into the device in the same amount of time and, therefore, more voltage potential is generated from $V = L \times di/dt$.

Figure 2 is an oscilloscope view of ground bounce that shows the device ground and one of many simultaneously switching outputs. The top waveform is one of the switching I/O pins, and the bottom waveform is the quiet pin, or the I/O pin driving out low. The ground bounce is evident as the device ground (quiet pin) bounces when the outputs switch from `1` to `0`. Also, the ground bounces slightly when the outputs switch from `0` to `1` due to small switching currents in the device. This switching noise is so small that it is not a problem.

Figure 2. Ground Bounce)



It is important to understand the mechanism for measuring the device ground, which is to monitor an I/O driving out low, commonly referred to as a quiet pin. Since ground pins are connected directly to the board ground, monitoring a ground pin will represent the board ground, not the internal device ground.

Problems occur when the amplitude of the ground bounce becomes too large. Signals may be misinterpreted because the relative ground levels are different for the driving device and the receiving device. This discrepancy can cause a logic `0` to be interpreted as a logic `1`.

Take the example of a 3.3-V transistor-to-transistor logic (TTL) system, which has a maximum V_{IL} (maximum voltage for input low) threshold of 0.8 V and minimum V_{IH} (minimum voltage for input high) threshold of 2.0 V. A device with 1.1 V of ground bounce outputs a logic low signal to another device not exhibiting ground bounce. The downstream device receives a 1.1-V signal, which is above the V_{IL} threshold and could be misinterpreted as a logic `1`. This misinterpretation occurs because the driving device exhibits ground bounce resulting in a logic low output of 1.1 V above the ground of the board and, therefore, 1.1 V above the ground of the receiving device.

Another problem occurs on the input side of the device that exhibits ground bounce. The problem can occur when one input pin is near a bus of SSOs. If a device exhibits 1.1 V of ground bounce, then a logic `1` input signal could be misinterpreted as a logic `0`, since the difference between the ground and the input signal shrinks by 1.1 V. For a 3.3-V TTL system, the maximum voltage of a logic `1` input is V_{CC}-1.4 V, or 1.9 V, which is below the minimum V_{IH} and above the maximum V_{IL}. This signal could be interpreted as a logic `0` or `1` because the voltage is between the maximum V_{IL} and the minimum V_{IH}.

V_{CC} Sag

V_{CC} sag occurs in the same manner as ground bounce, but it is more prevalent when the I/O pins switch from `0` to `1` and affects the internal V_{CC} of the device instead of the GND.

Design Methods to Minimize Ground Bounce & V_{CC} Sag

Design methods that reduce the inductance and reduce the rate of change of current decrease the amount of ground bounce and V_{CC} sag. These design methods include the use of:

- Flip Chip device packages
- Slow slew rate
- Limit the number of simultaneously switching output (SSOs) per I/O bank
- Spread out SSOs
- Programmable GND and V_{CC} pins
- Out-of-phase simultaneously switching output (SSOs) using phase-locked loops (PLLs)
- Out-of-phase simultaneously switching output (SSOs) using programmable output delay option
- Series termination resistors
- Series-RC parallel terminations
- Decoupling capacitors

Altera conducted tests on a board with an APEX™ EP20K100EFC324-1X device to determine how much each design method improved ground bounce and V_{CC} sag. The results for each test are shown in Table 1.

Many variables, including board design, board layout, load on the I/O pins, package type, and device density, can affect ground bounce and V_{CC} sag. The results from this testing should be considered as a guideline only and not taken as characteristic of every application.

The results are summarized in Table 1. The remainder of this white paper describes the tests in more detail.

Table 1. Ground Bounce and V_{CC} Sag Test Results

Design Method (APEX EP20K100EFC324-1X)	% Improvement	
	GND Bounce	V_{CC} Sag
Device package (Flip Chip vs. wire-bonded)	72	58
Slow slew rate	65	61
Half the number of SSOs	11 to 35	12 to 31
Tri-state every other I/O pin (- Z - I/O- Z - I/O - Z -)	13	28
Tri-state every third I/O pin (- Z - I/O - I/O - Z - I/O - I/O - Z -)	7	25
Programmable GND or V_{CC} on every other I/O pin. Programmable GNDs and V_{CC} s are connected to board GND or V_{CC}.(- V_{CC} - I/O - GND - I/O - V_{CC} -)	45	49
Programmable GND or V_{CC} on every other I/O pin. Programmable GNDs and V_{CC} s are not connected to board GND or V_{CC} and have a 7.5-pF load.	24	22
Programmable GND or V_{CC} on every 3rd I/O pin. Programmable GNDs and V_{CC} s are connected to board GND or V_{CC}. (- V_{CC} - I/O - I/O - GND - I/O - I/O - V_{CC} -)	41	22
Programmable GND or V_{CC} on every third I/O pin. Programmable GNDs and V_{CC} s are not connected to board GND or V_{CC} and have a 7.5-pF load.	71	25
Programmable GND or V_{CC} on every third I/O pin with a 10-Ω series resistor on each I/O pin. Programmable GNDs and V_{CC} s are not connected to board GND or V_{CC} and have a 7.5-pF load.	68	31
PLL clock drives every other I/O pin (clock shift of 341 ps)	12	24
Programmable output delay (t_{co} 520 ps different)	12	25
10-Ω series termination resistor (interpolated)	46	12
Series-RC parallel termination (100 pF and 50 Ω)	47	31

Flip Chip Device Packages

The device package type significantly affects the inductance value. Ball-grid arrays (BGAs) have far less inductance than leaded devices, such as quad flat packs (QFPs) and pin-grid arrays (PGAs). Also, different types of BGAs have varying inductances depending on the internal structure. For example, the inductance of a Flip Chip BGA is far less than that of a wire-bonded BGA because the die in a Flip Chip BGA is face down, which allows short connections to the balls. The die in wire-bonded BGA and QFP packages is face up with tiny wires from the I/O pins to the die. Therefore, with other factors being equal there is far less ground bounce in a Flip Chip package than a wire-bonded package.

Test

The same ground bounce and V_{CC} sag tests were performed on a wire-bonded EP20K100EFC324-1X device and a Flip Chip FBGA EP20K400EFC672-1X device. Both devices have approximately the same ratio of power pins to I/O pins.

Results

Using the Flip Chip package instead of the wired-bonded package improved the ground bounce and V_{CC} sag on average 72% and 58%, respectively. The die size has a small effect on ground bounce, which increases with increased die size. Therefore, the results for the Flip Chip device are a little deflated as compared to the wire-bonded devices.

Slow Slew Rate

Slew rate refers to the edge rate of an output pin. Fast or slow slew rate is software selectable on a pin-by-pin basis for Altera devices. By default, all Altera device I/O pins are set to a fast slew rate to obtain the fastest clock-to-out timing. Slowing down the slew rate reduces the current draw and, therefore, greatly decreases ground bounce and V_{CC} sag.

Test

Select slow slew rate instead of fast slew rate for all the switching pins on the EP20K100EFC324-1X device.

Results

Ground bounce and V_{CC} sag improved 65% and 61%, respectively.

Limit the Number of Simultaneously Switching Outputs (SSOs) per I/O Bank

Many Altera devices have several I/O banks each with separate power pins, which allow different V_{CC} levels and I/O standards to be used on the same chip. Limiting the number of SSOs per bank helps keep the current per power pin at a minimum. As the number of SSOs increases, the amount of ground bounce and V_{CC} sag steadily increases and then starts to flatten out due to supply current limitations of the device. This causes the percent reductions in ground bounce and V_{CC} sag to have a wide range when reducing the number of SSOs.

Test

Reduce the number of SSOs by 50%.

Results

Ground bounce and V_{CC} sag improved 11% to 35% and 12% to 31%, respectively, when varying the number of SSOs. As the number of SSOs increases, the amount of ground bounce and V_{CC} sag increases and then flattens (and in some cases decreases). This characteristic is due to the output buffers reaching their maximum current-carrying capacity. The range in improvement for ground bounce and V_{CC} sag for this test is due to this characteristic.

Spread Out Simultaneously Switching Output (SSO) Pins

Spreading out the simultaneously switching output pins in the I/O bank is another technique that helps lower the change in current.

Test

This test evaluates the effect two different switching I/O patterns have on ground bounce and V_{CC} sag.

- Place a tri-stated pin between every switching I/O pin. The I/O pin configuration is - Z - I/O - Z - I/O - Z -.
- Place a tri-stated pin between every 3rd I/O pin. The I/O pin configuration is - Z - I/O - I/O - Z - I/O - I/O - Z -.

Results

- For the first test, ground bounce and V_{CC} sag improved 13% and 28%, respectively.
- For the second test, ground bounce and V_{CC} sag improved 7% and 25%, respectively.

Programmable GND & V_{CC} Pins

One feature of Altera devices that helps reduce ground bounce and V_{CC} sag and increase noise immunity is programmable GND and V_{CC} pins, which are I/O pins internally connected to the ground and V_{CC} of the device. The programmable GND/V_{CC} option is available on a pin-by-pin basis. All unused I/O pins may optionally drive out ground, which is recommended for applications susceptible to noise and ground bounce problems. Adding programmable GND and V_{CC} pins helps decrease the overall inductance by offering more paths to ground and helps decrease the return loop inductance by having the grounds closer to the switching I/O pins.

Test

These tests evaluate the effect of different programmable GND and V_{CC} configurations. In each test the programmable power pins alternate between GND and V_{CC}. The 7.5 pF load emulates a typical TTL load.

1. Connect every other programmable GND and V_{CC} I/O pin to GND or V_{CC} on the board. The I/O pin configuration is - V_{CC} - I/O - GND - I/O - V_{CC} -.
2. Connect every other programmable GND and V_{CC} I/O pin to a 7.5 pF load.
3. Connect every 3rd programmable GND and V_{CC} I/O pin to GND or V_{CC} on the board. The I/O pin configuration is - V_{CC} - I/O - I/O -GND - I/O - I/O - V_{CC} -.
4. Connect every 3rd programmable GND and V_{CC} I/O pin to a 7.5 pF load.

Results

The results for each test are as follows:

1. Having every other programmable GND and V_{CC} I/O pin connected to a board GND or V_{CC} on the board improved ground bounce and V_{CC} sag by 45% and 49%, respectively.
2. Having every other programmable GND and V_{CC} I/O pin connected to a 7.5 pF load improved ground bounce and V_{CC} sag by 24% and 22%, respectively.
3. Having every 3rd programmable GND and V_{CC} I/O pin connected to GND or V_{CC} on the board improved ground bounce and V_{CC} sag by 42% and 22%, respectively.
4. Having every 3rd programmable GND and V_{CC} I/O pin connected to a 7.5 pF load improved ground bounce and V_{CC} sag by 71% and 25%, respectively.

Out-of-Phase Simultaneously Switching Outputs (SSOs) Using PLLs

Altera PLLs can be used to help reduce ground bounce and V_{CC} sag. PLLs can shift the clock feeding a portion of the output registers, so only a portion of the registers switch simultaneously. By lowering the number of SSOs, less current flows through the power pins. Altera recommends that the shifted clock feed every other output pin in the bus in order to spread out the simultaneously switching pins among the ground and V_{CC} pins.

Test

Use a PLL to shift the clock so there is 341 ps difference between the two clocks feeding the registers that drive switching I/O pins. The shifted clock feeds the register feeding every other switching I/O pin.

Results

Ground bounce and V_{CC} sag improved by 12% and 24%, respectively.

Out-of-Phase Simultaneously Switching Outputs (SSOs) Using Programmable Output Delay

APEX 20KE devices have a programmable output delay between the output register in the I/O cell and the I/O pin. By turning on the programmable delay for every other SSO, half the outputs switch slightly later. The change in current, di/dt, is approximately half, since only half the outputs are switching simultaneously. Turn on the programmable delay for every other output to spread out the SSO around each power pin. This helps reduce the change in current through each power pin and the amount of ground bounce and V_{CC} sag. The programmable output delay and the PLL accomplish the same goal, except that the PLL gives the designer more control of the amount of delay.

Test

Turn on the programmable delay for every other SSO. The Quartus® II software reported a 520-ps difference in t_{co} for every other register.

Results

Ground bounce and V_{CC} sag improved 12% and 25%, respectively.

Series Termination Resistors

While series termination resistors help control the reflections on the signals; adding series resistors to the SSOs is another method for reducing ground bounce and V_{CC} sag by limiting the current. The edge rate slows down slightly, but this is often acceptable when using a small resistor (10 Ω to 33 Ω). The benefit of the reduction in ground bounce and V_{CC} sag often far outweighs the added delay.

Refer to the Series Termination section of *Application Note 75 (High-Speed Board Design)* for a schematic of this termination scheme.

Test

These tests evaluate the effect of termination resistors on ground bounce and V_{CC} sag.

- Place a 10-Ω series resistor on every switching output.
- Place a 10-Ω series resistor on all SSOs with every 3rd I/O pin as a programmable GND or V_{CC}.

Results

- With a 10-Ω series resistor on every switching output, ground bounce and V_{CC} sag improved 46% and 12%, respectively. The resistor added 50-ps delay on the output pins.
- With a 10-Ω series resistor on all SSOs with every 3rd I/O pin as a programmable GND or $V_{CC,}$ ground bounce and V_{CC} sag improved 45% and 49%, respectively. The resistor added 50-ps delay on the output pins.

Series-RC Parallel Termination

In a parallel termination scheme, a resistor and capacitor network is used as a terminating impedance. The terminating resistor is equal to Z_o, which is usually 50-Ω.The capacitor must be greater than 100pF. The capacitor blocks low-frequency signals while passing high-frequency signals. Therefore, the DC loading effect of the terminating resistor does not have an impact on the driver.

Refer to the Series-RC Parallel Termination section of *Application Note 75 (High-Speed Board Design)* for a schematic of this termination scheme.

Test

Use a 100-pF capacitor and a 50-Ω terminating resistor.

Results

Ground bounce and V_{CC} sag improved 47% and 31%, respectively.

General Recommendations

The following are some general recommendations to reduce ground bounce and V_{CC} sag in designs.

Synchronous vs. Asynchronous

Settling time is an important parameter that affects ground bounce and V_{CC} sag. Settling time is the amount of time the signal stays above the maximum threshold voltage for a logic `0`. For a synchronous signal, as long as the signal is sampled after the signal settles, the signal is interpreted correctly. Any glitch on an asynchronous signal triggers the receiving device. Therefore, whenever possible use synchronous signals.

Use Low Voltage Differential Signal (LVDS)

Designers can use I/O terminations to help minimize ground bounce. One popular I/O standard for high-speed applications is low-voltage differential signaling, due to the combined advantages of high bandwidth and high immunity to noise. Any noise in the system is common to both the positive and negative wires of the channel and, therefore, is filtered out by the differential input of the LVDS receiver.

Follow General Board Design Guidelines

For all designs it is recommended to use 0.1µF and 0.01 µF decoupling capacitors in parallel. An additional 0.001µF decoupling capacitor is highly recommended for designs that may be susceptible to ground bounce and V_{CC} sag.

When assigning the pin-out for each device, placement of SSOs should be taken into consideration. Always place them close to as many power pins as possible and, in extreme cases, sandwich them among the power pins and programmable GND and V_{CC} pins to reduce the current each power pin has to source or sink. This reduces the change in current for each power pin and thus reduces the amount of ground bounce and V_{CC} sag ($V = L \times di/dt$).

When adding the vias for the decoupling capacitors, place them as close to the capacitor pad as possible and use as large as possible vias. Both of these design techniques help minimize the inductance. Overlapping the pad and the via avoids the necessity of a trace. When doing this, it is important not to overlap too far because the solder from the pad may sink into the via and the capacitor will not adhere to the pad. Consult the PCB manufacturer for recommendations.

Refer to *Application Note 75 (High-Speed Board Design)* for more detailed recommendations on high-speed board design.

Conclusion

Ground bounce and V_{CC} sag are well-known in the semiconductor industry. Many design methods reduce them. Since ground bounce and V_{CC} sag go hand-in-hand, it is best to implement techniques for minimizing both. It is important to understand these analog issues when designing high-speed digital systems. With the proper board design practices and understanding of the phenomena, ground bounce and V_{CC} sag can be minimized in order to preserve signal integrity.

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